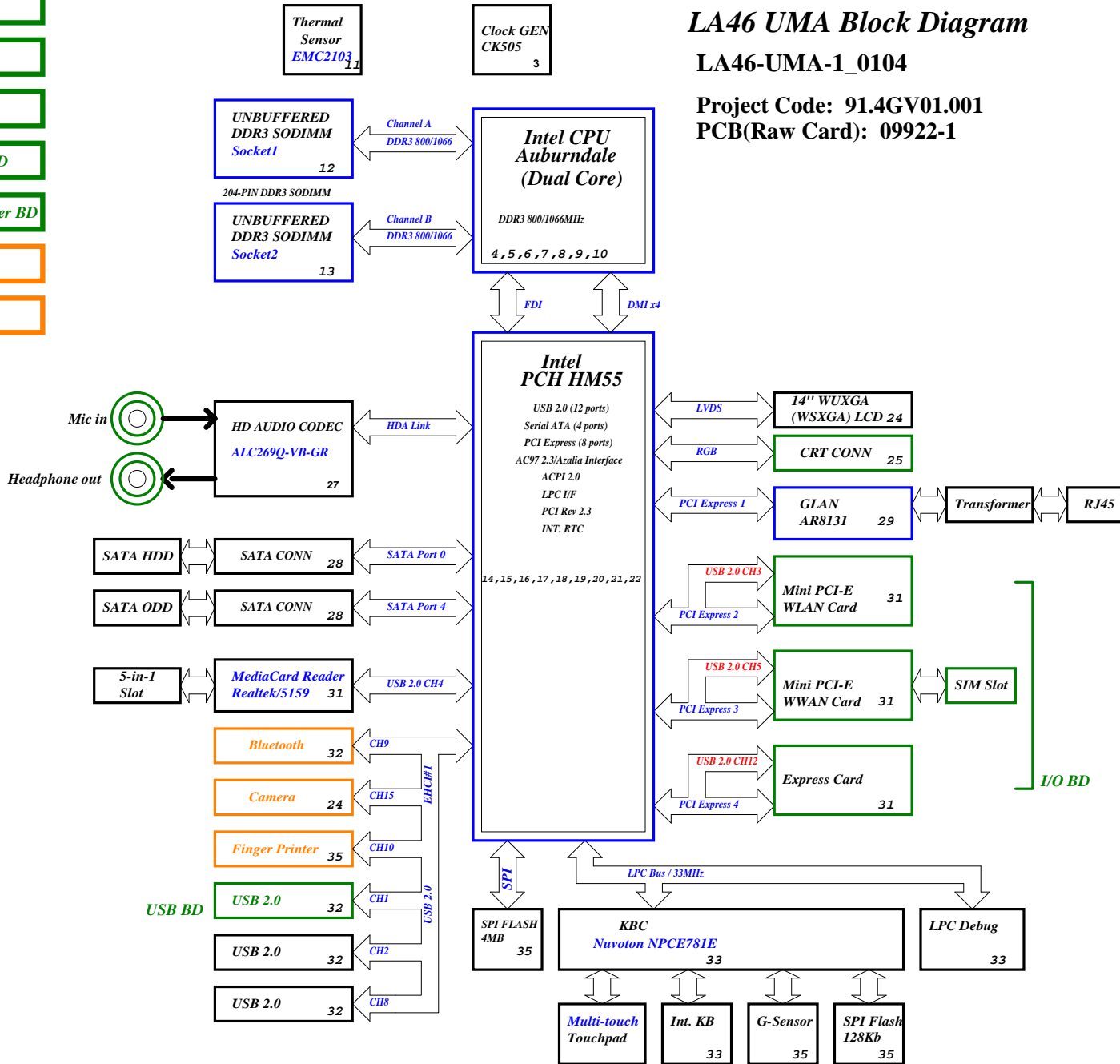


- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- AV BD
- BT BD



PCB LAYER	
L1:	Top
L2:	VCC
L3:	Signal
L4:	Signal
L5:	GND
L6:	Bottom

CPU DC/DC ISL62882 38, 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

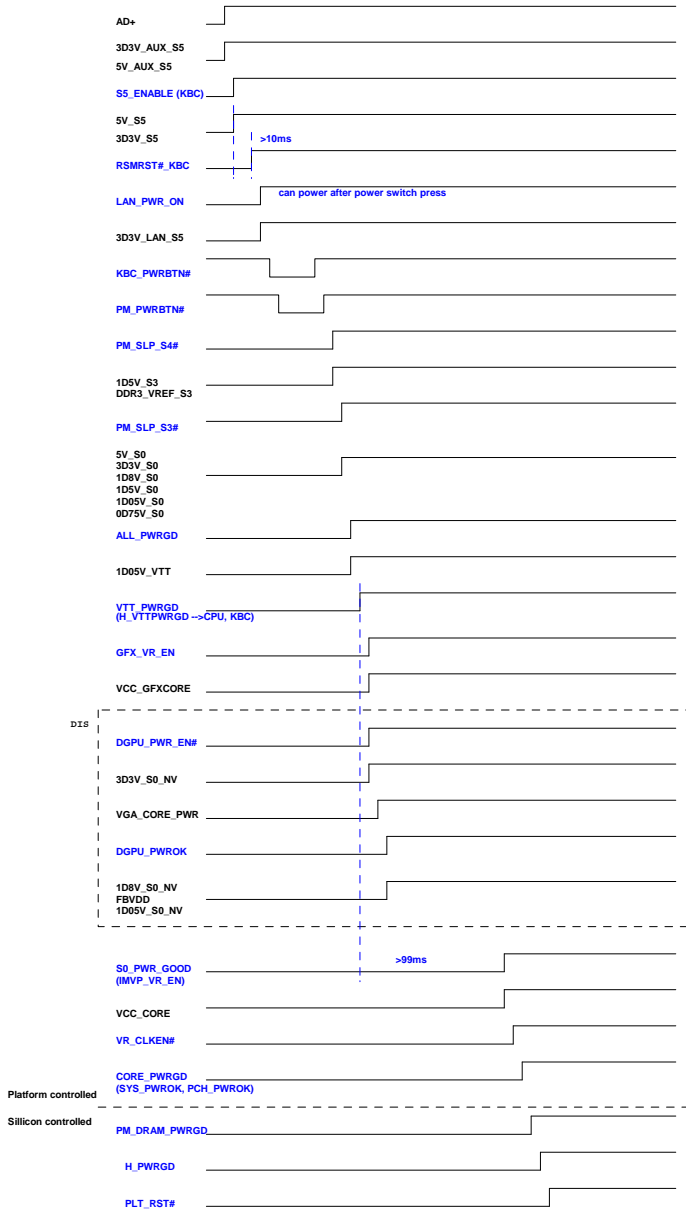
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.0k Ohm/5k resistor. Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCH Strapping

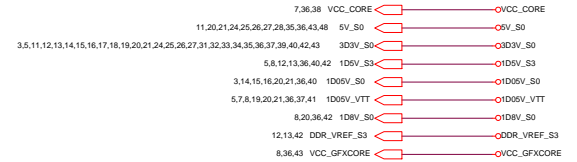
Name	Schematics Notes
SPKR	Reboot option at power-up. Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_VB#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ES1 compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SP1_MOSI	Enable ITPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable ITPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO133	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

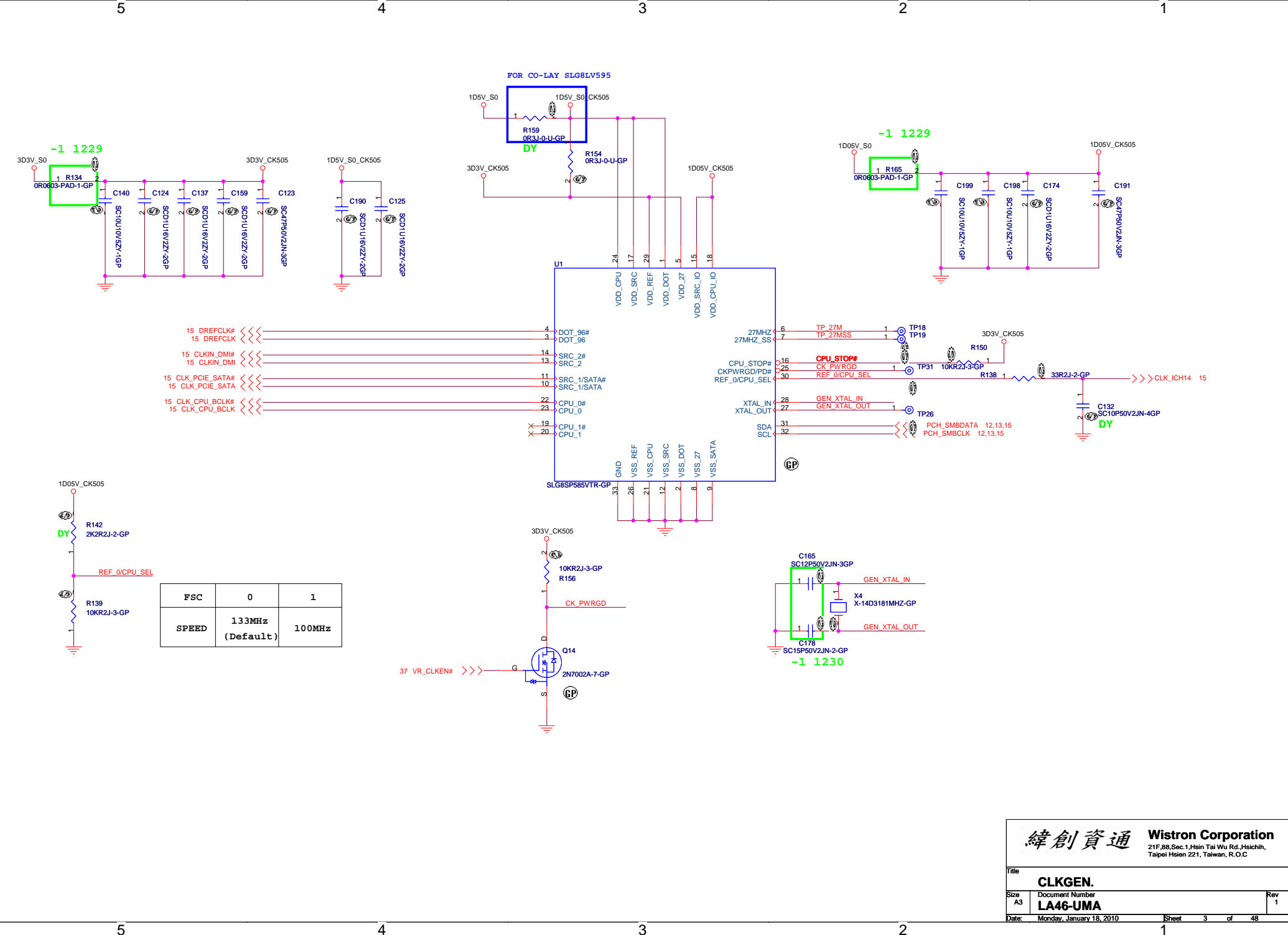
Sequence AC

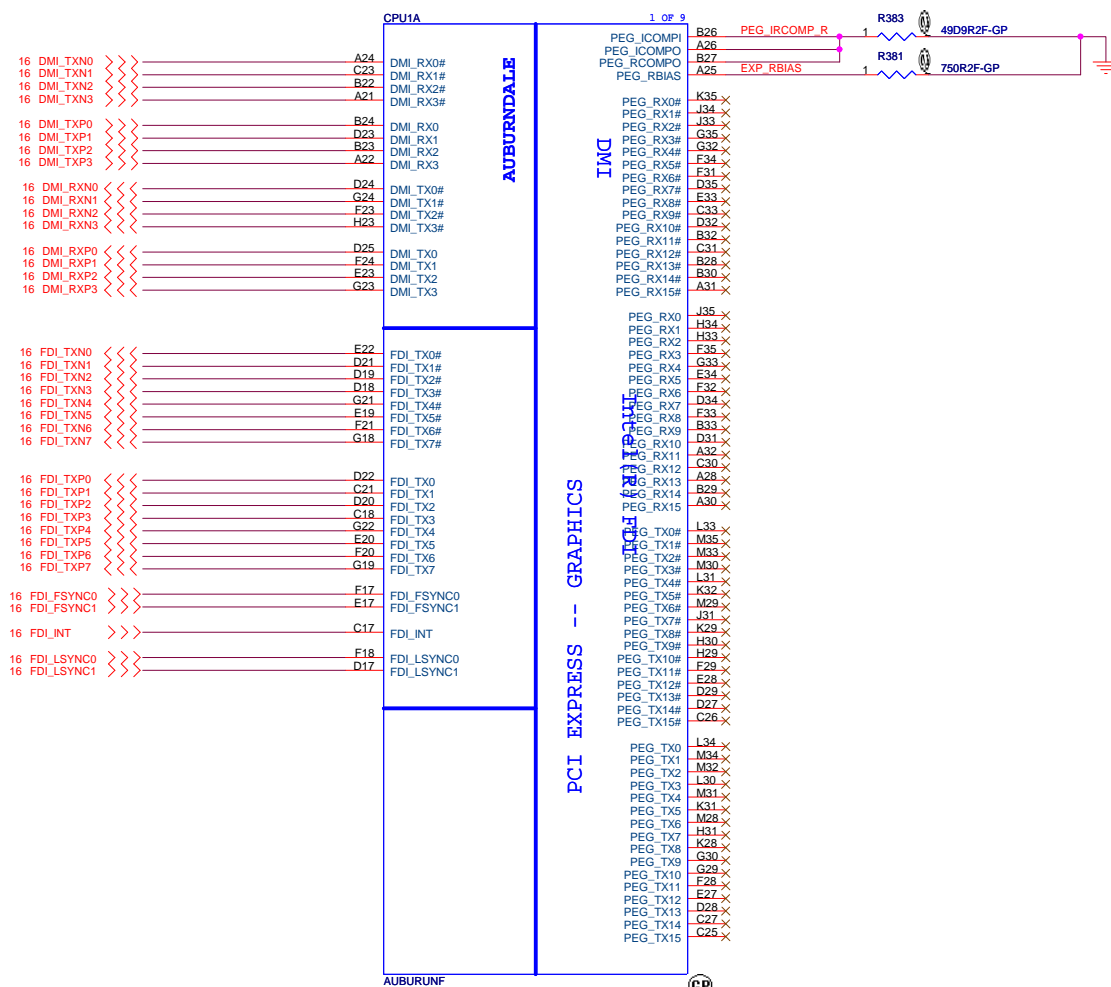


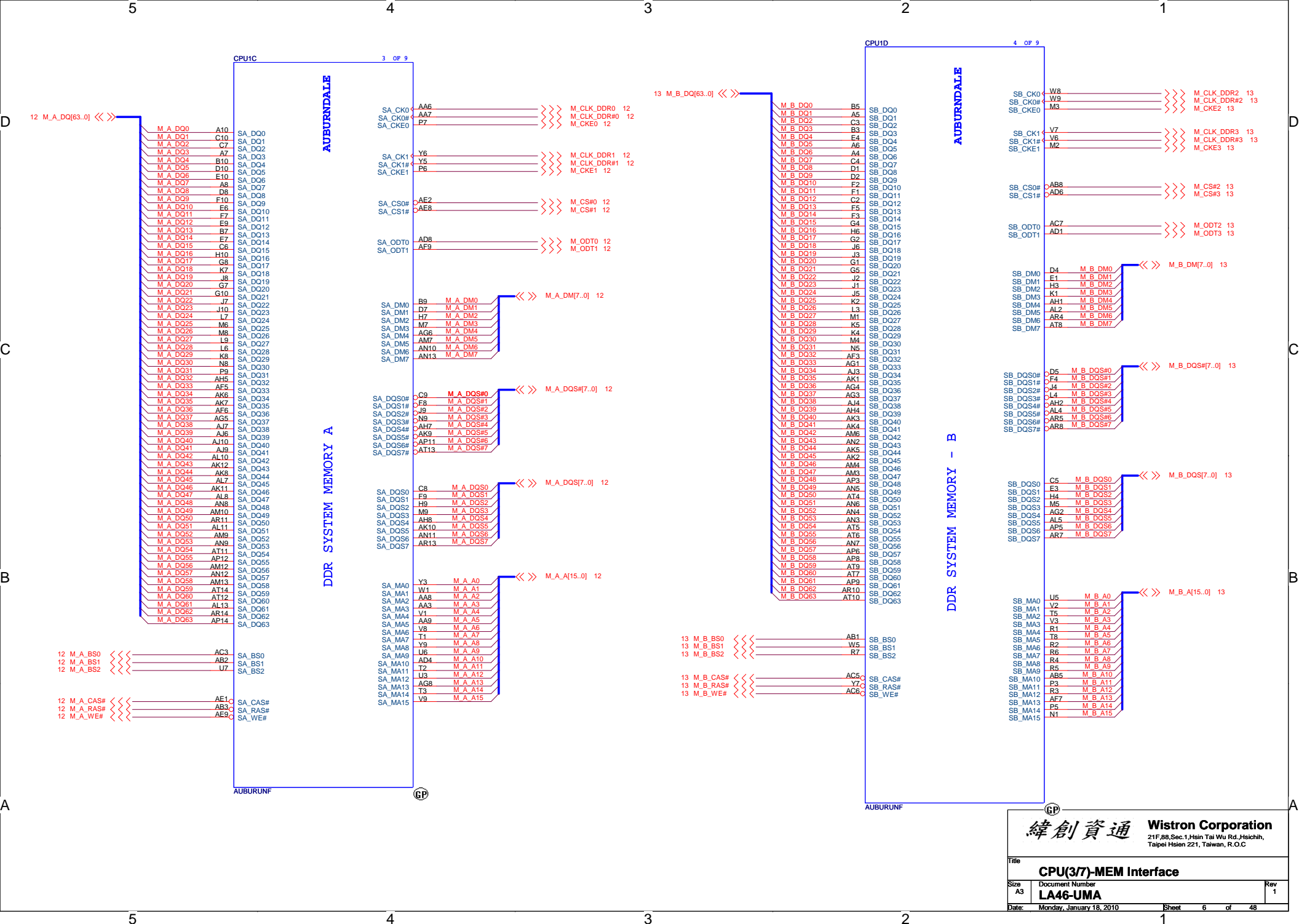
PLANAR_ID[1..0]

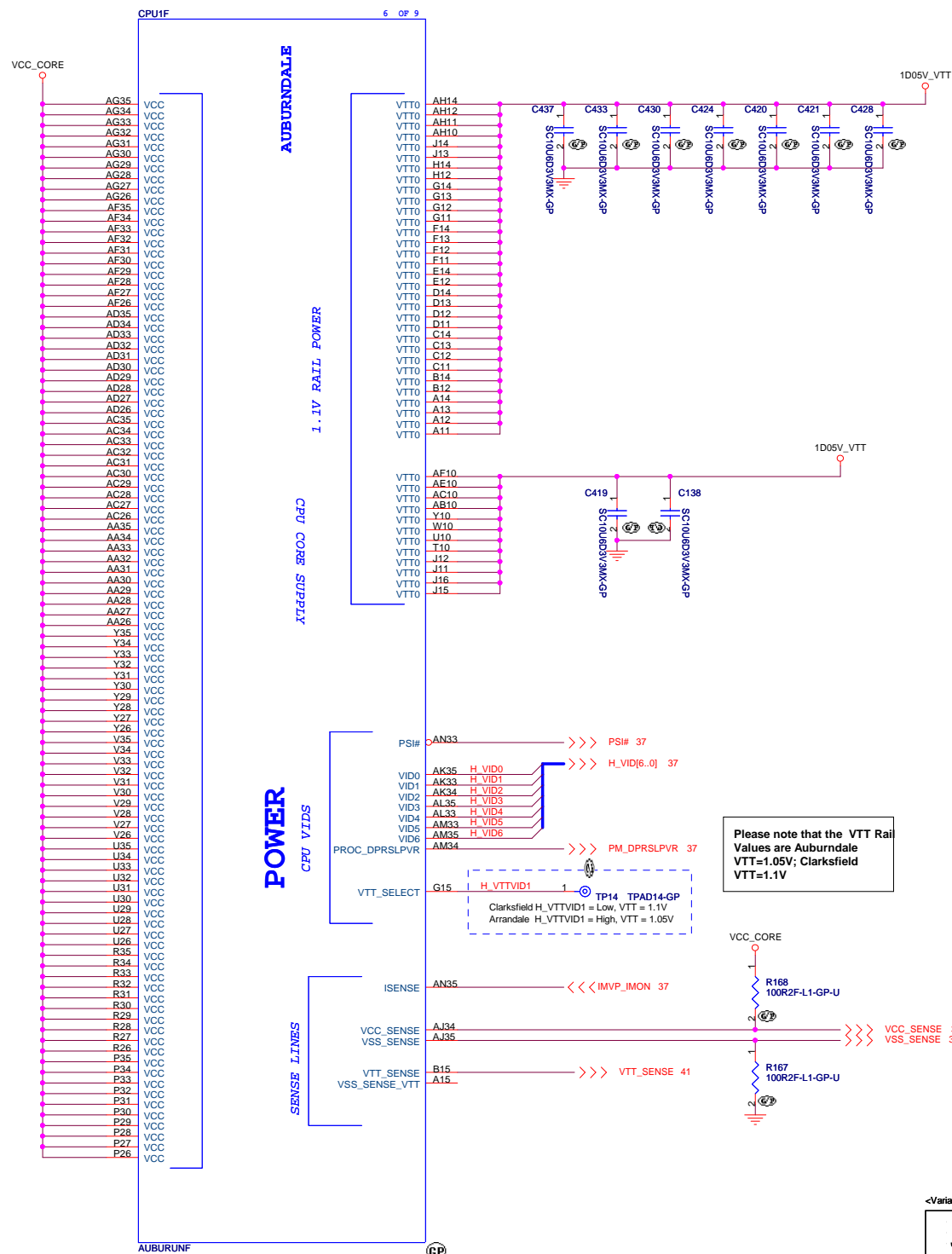
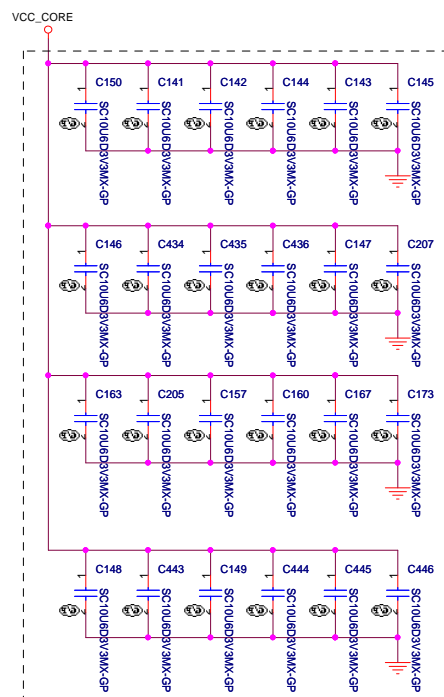
KBC GPin	31	23		
PLANAR_IDn	1	0	Planar ID Version	Planar PCB Version
	0	0	LA46_UMA- SA	SA
	0	1	LA46_UMA- SB	SB
	1	0	LA46_UMA- SC	SC
	1	1	LA46_UMA- 1	-1



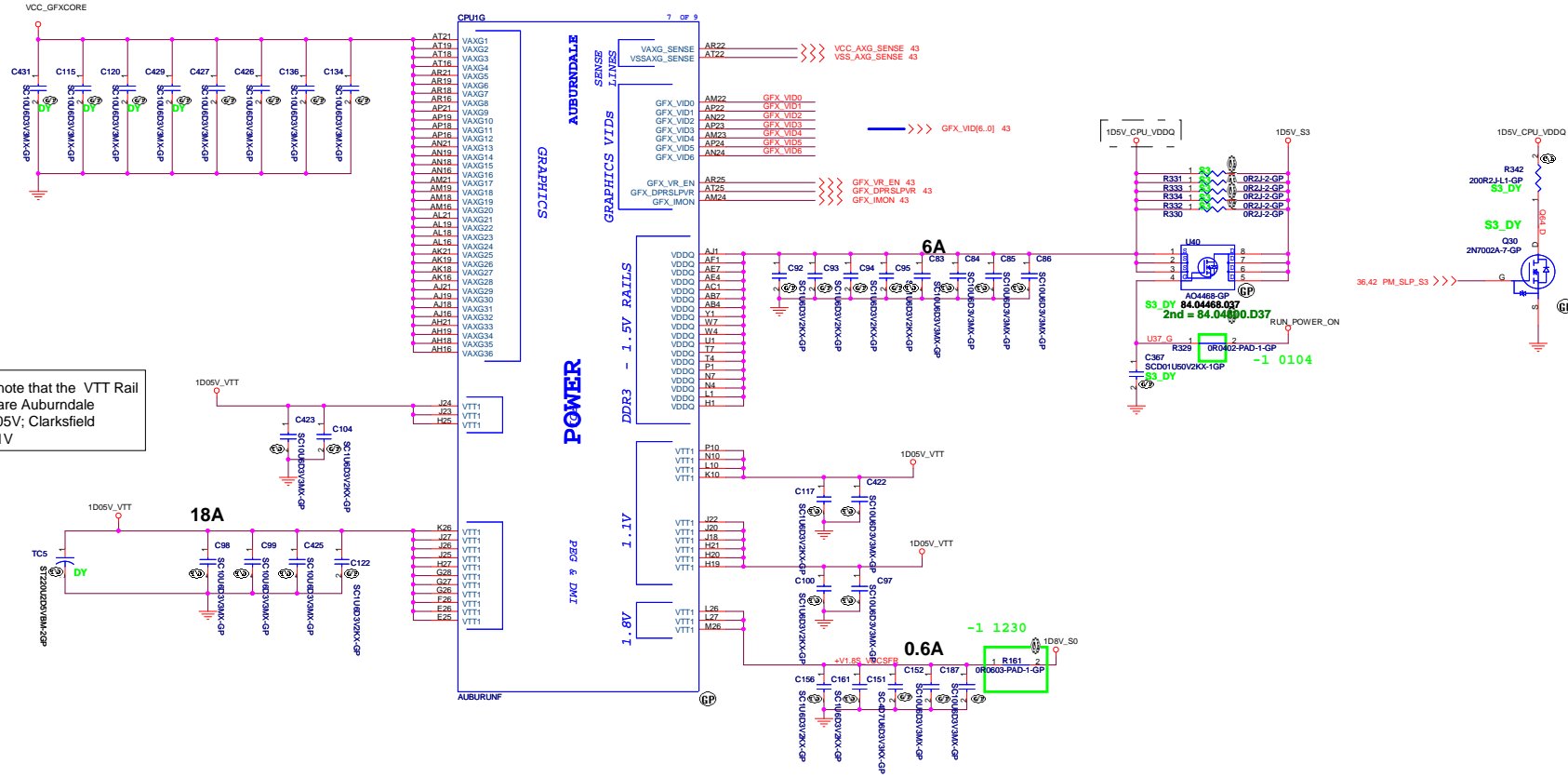


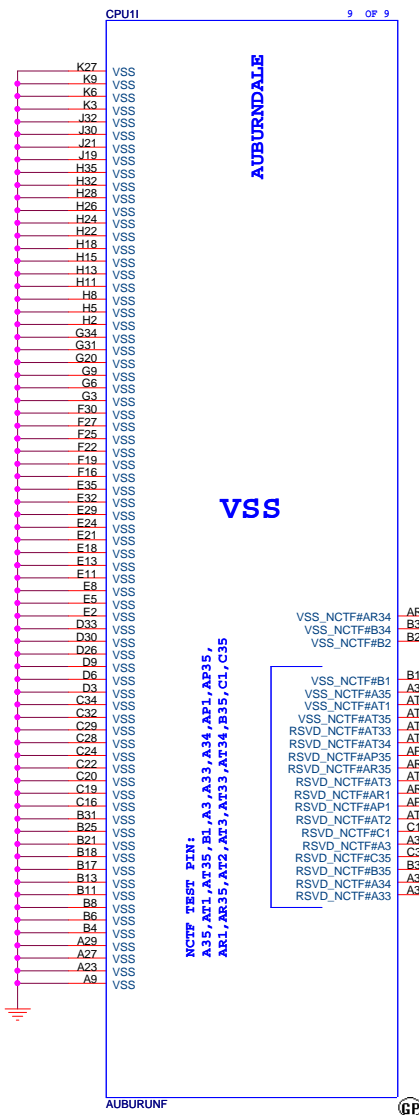
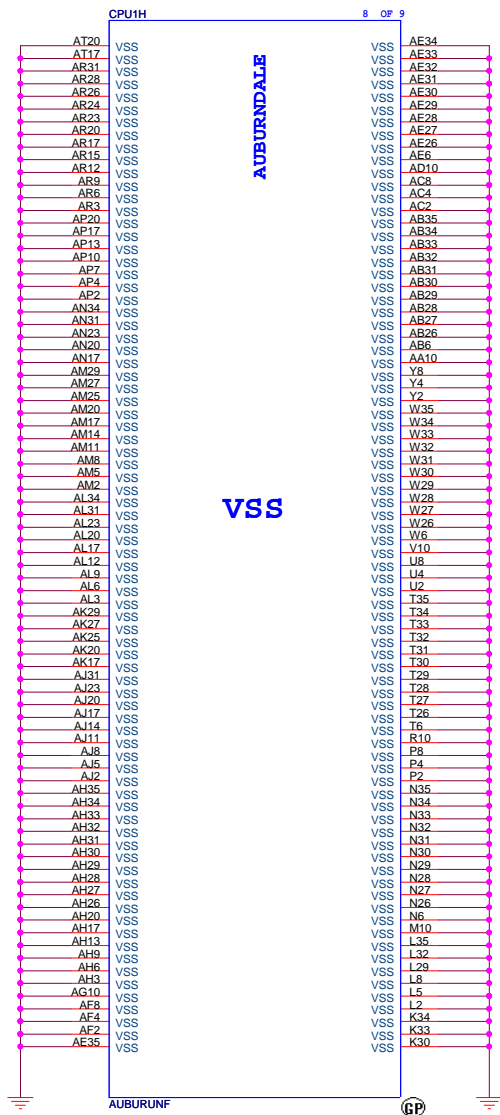


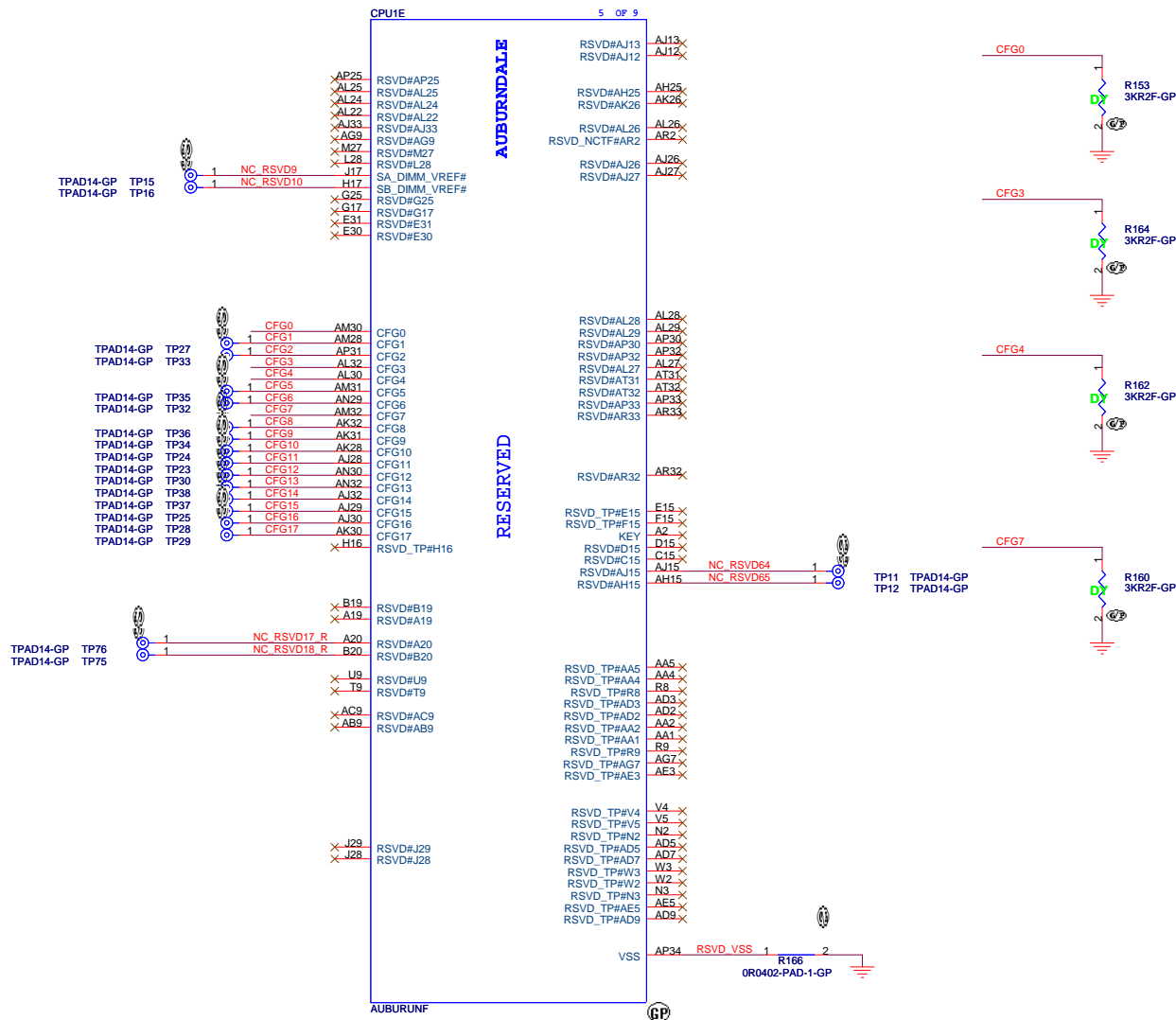




Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V







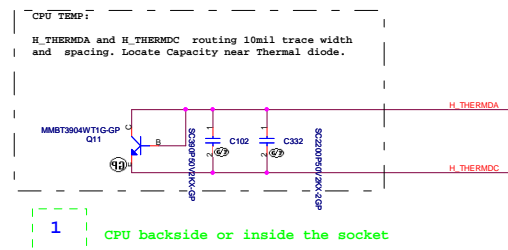
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

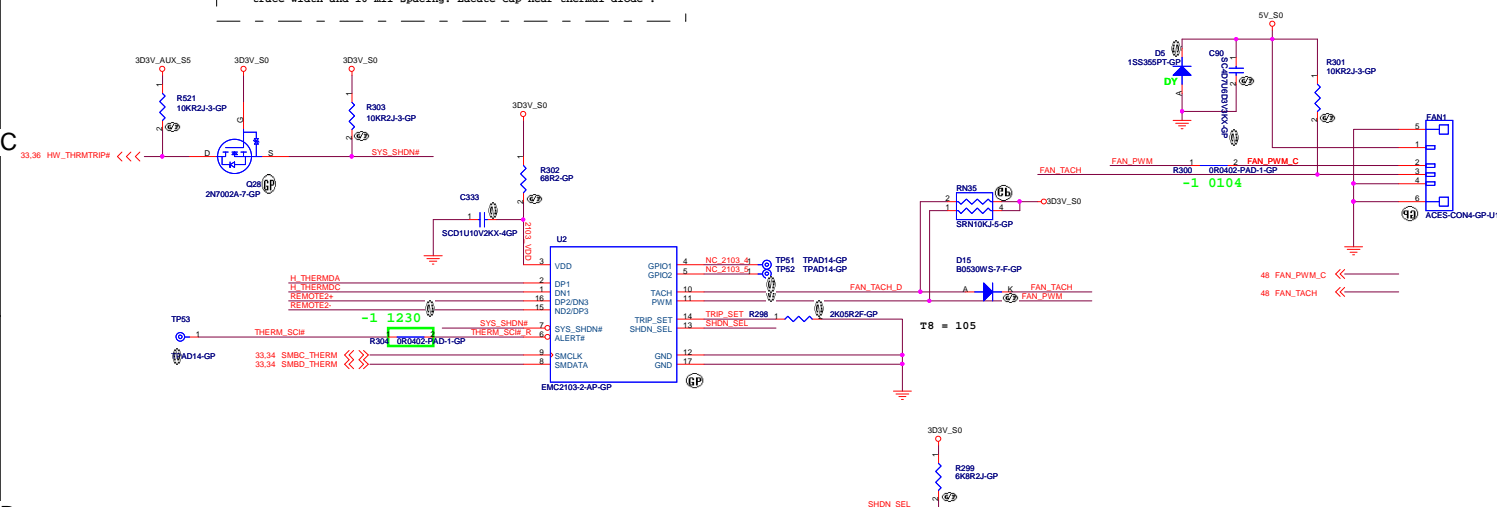
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

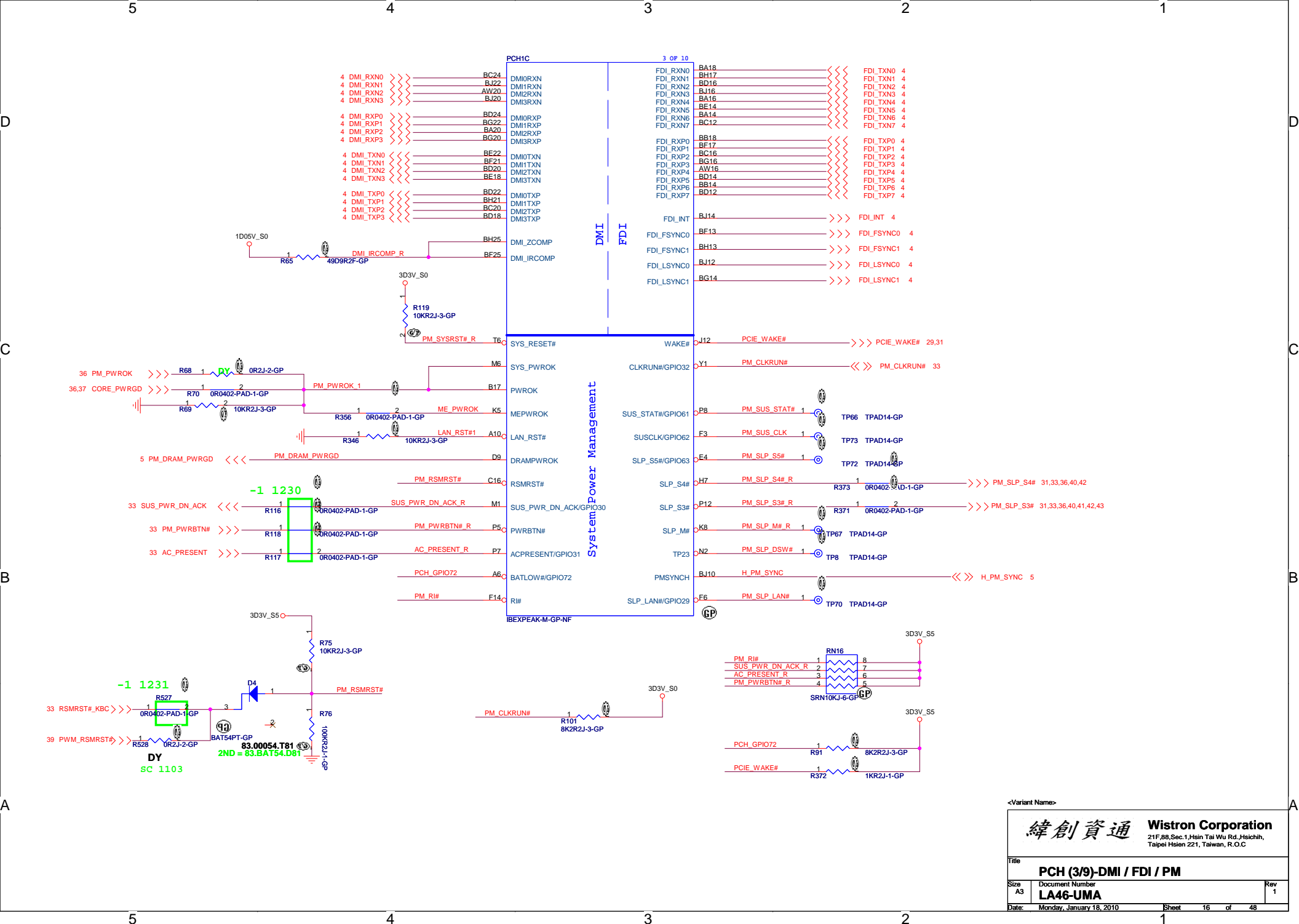
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title	
CPU(77)-RESERVED	
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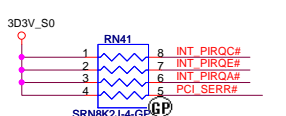
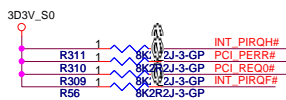
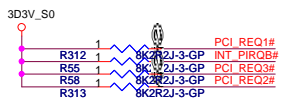
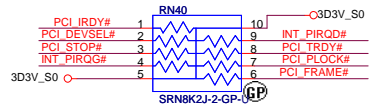


4 WIRE PWM Fan Control circuit

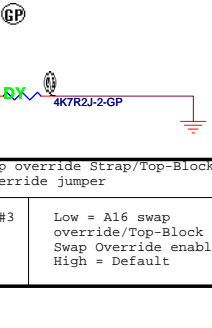
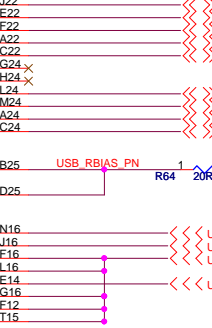
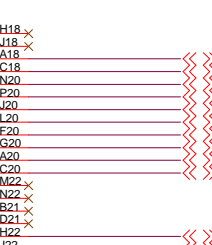
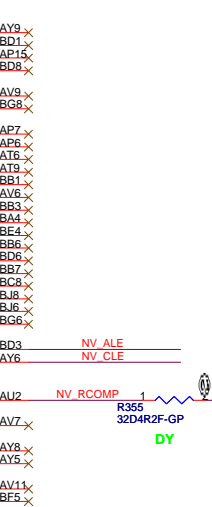
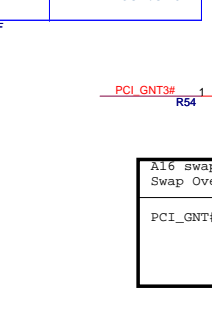
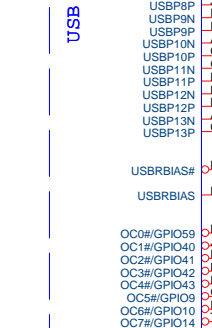
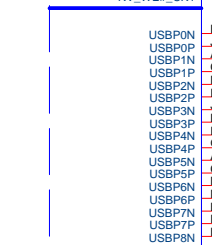
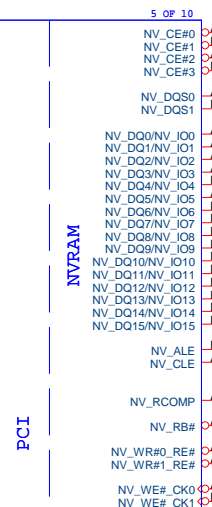
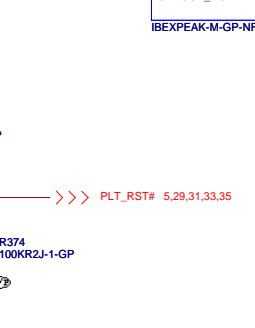
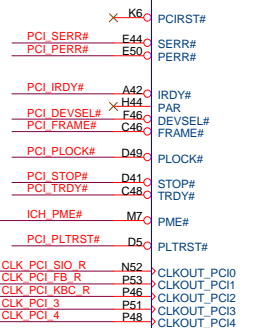
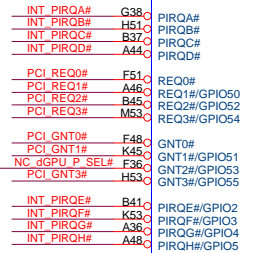
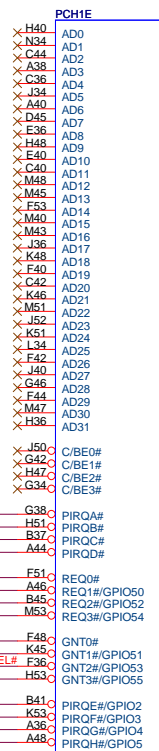
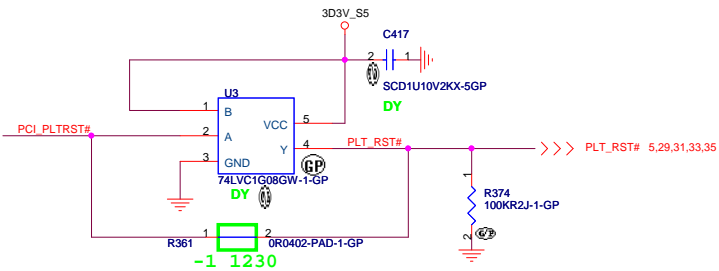
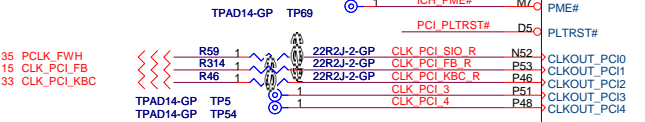




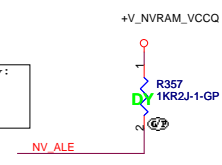
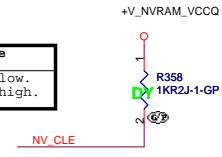




BOOT BIOS Strap		
PCI_GNT0#	PCI_GNT1#	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

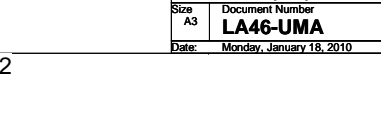
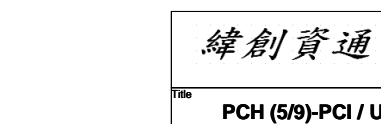
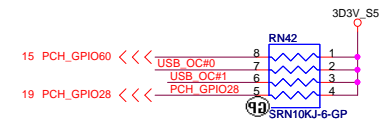


DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.



Danbury Technology:
Disabled when Low.
Enable when High.

Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

緯創資通
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C

Title
PCH (5/9)-PCI / USB

Size
A3

Document Number
LA46-UMA

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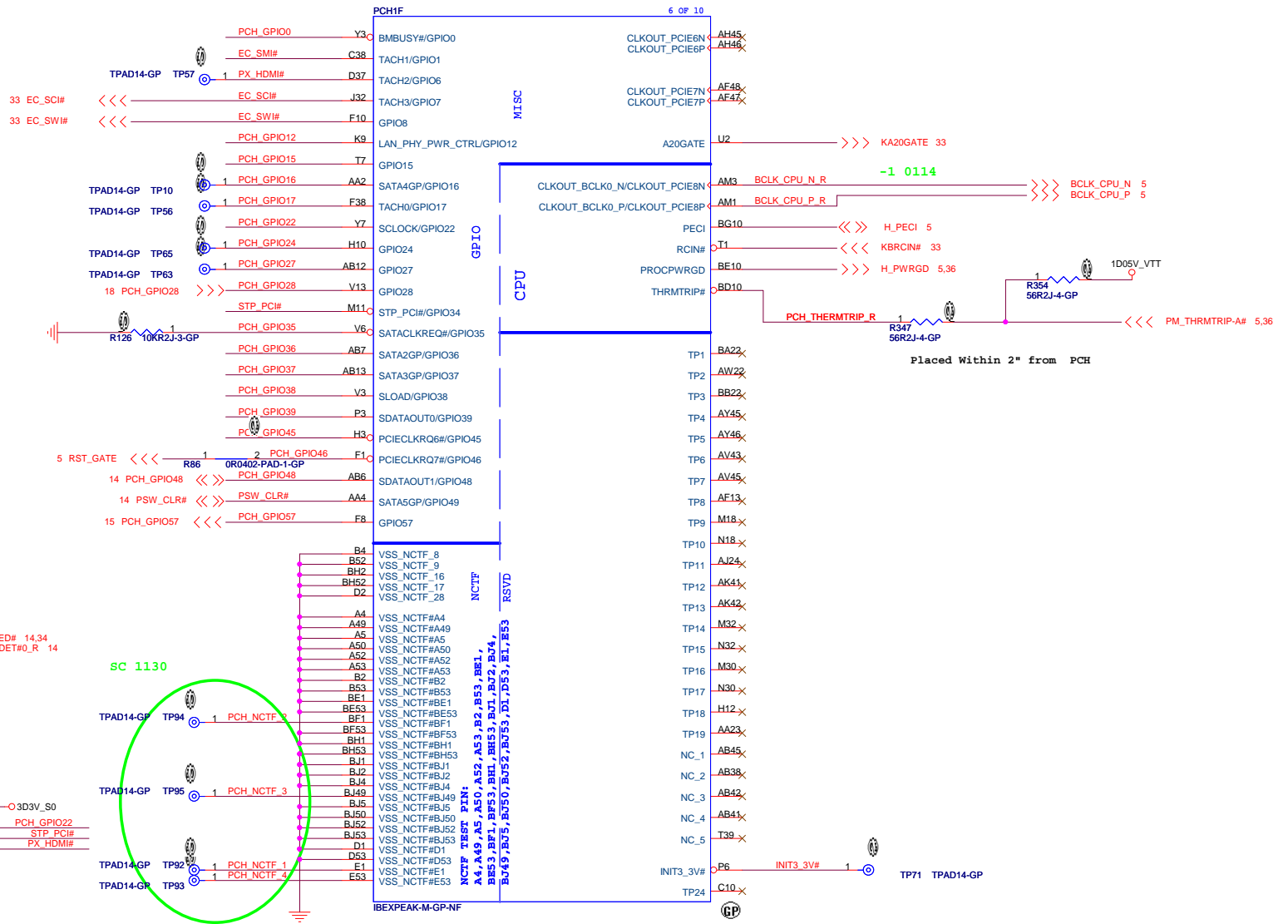
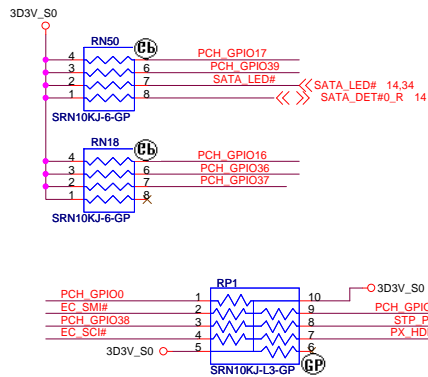
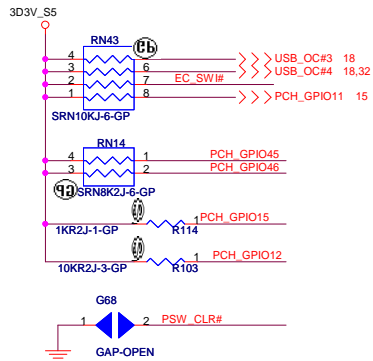
Sheet
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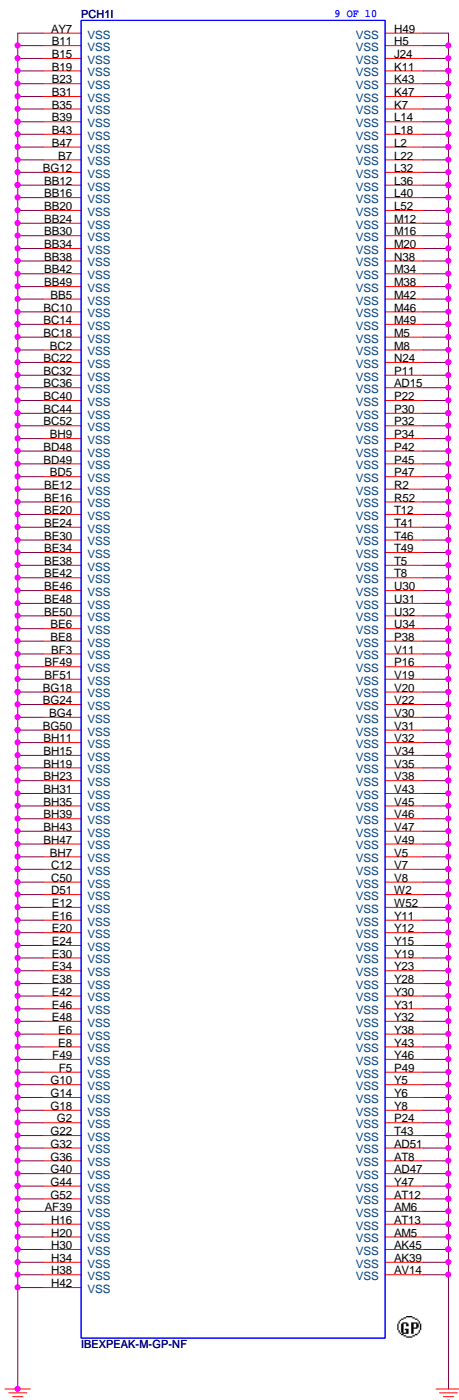
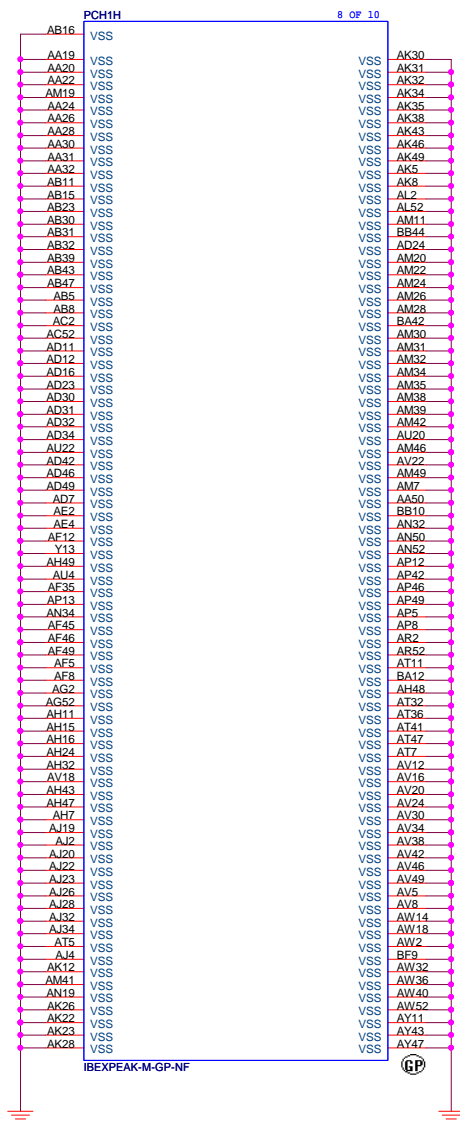
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

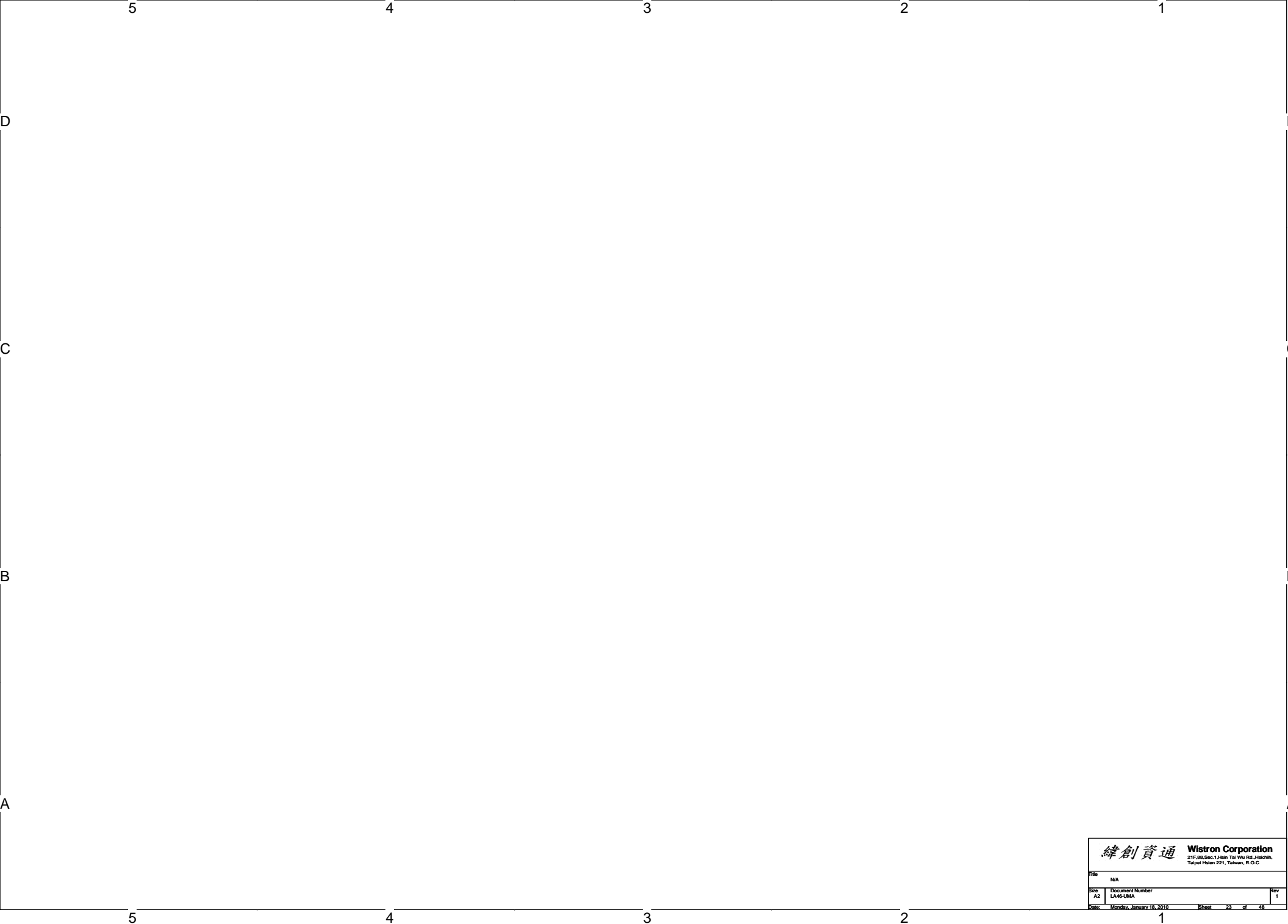
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title	
PCH (6/9)-GPIO/VSS_NCTF/RSVD	
Size	Document Number
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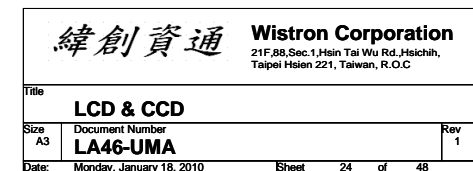


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21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C			
Title			
PCH (9/9)-VSS			
Size	Document Number		Rev
A3	LA46-UMA		1
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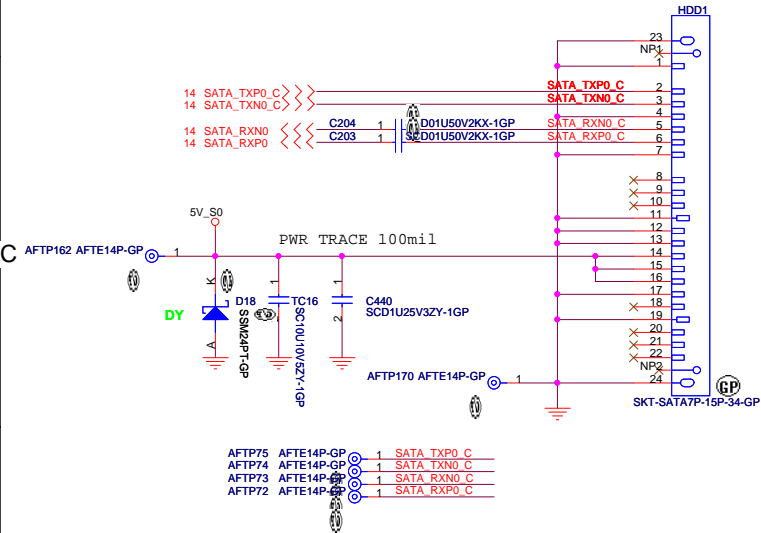
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Size	Document Number		Rev
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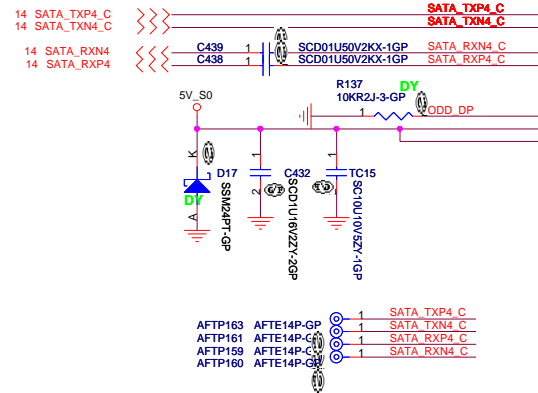




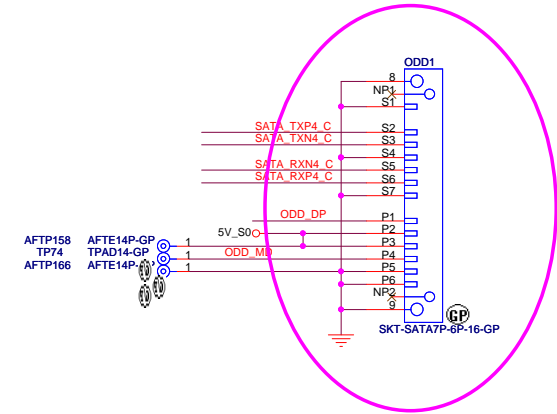
SATA Connector



ODD Connector

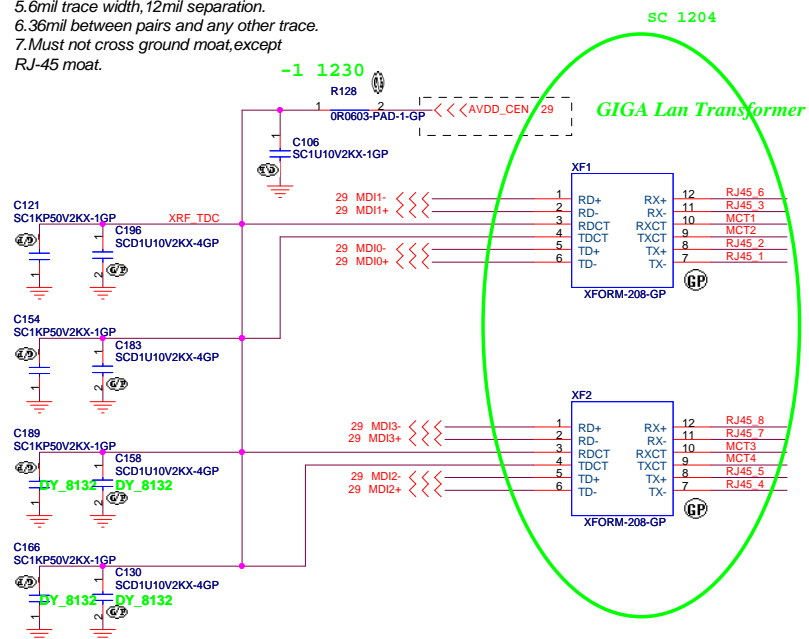


SB 1016

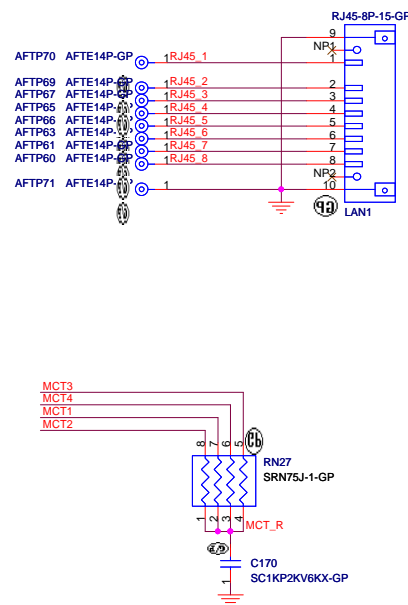


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HDD & ODD	
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



LAN Connector



<Variant Name>

緯創資通

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title
LAN CONN

Size
A3

Document Number
LA46-UMA

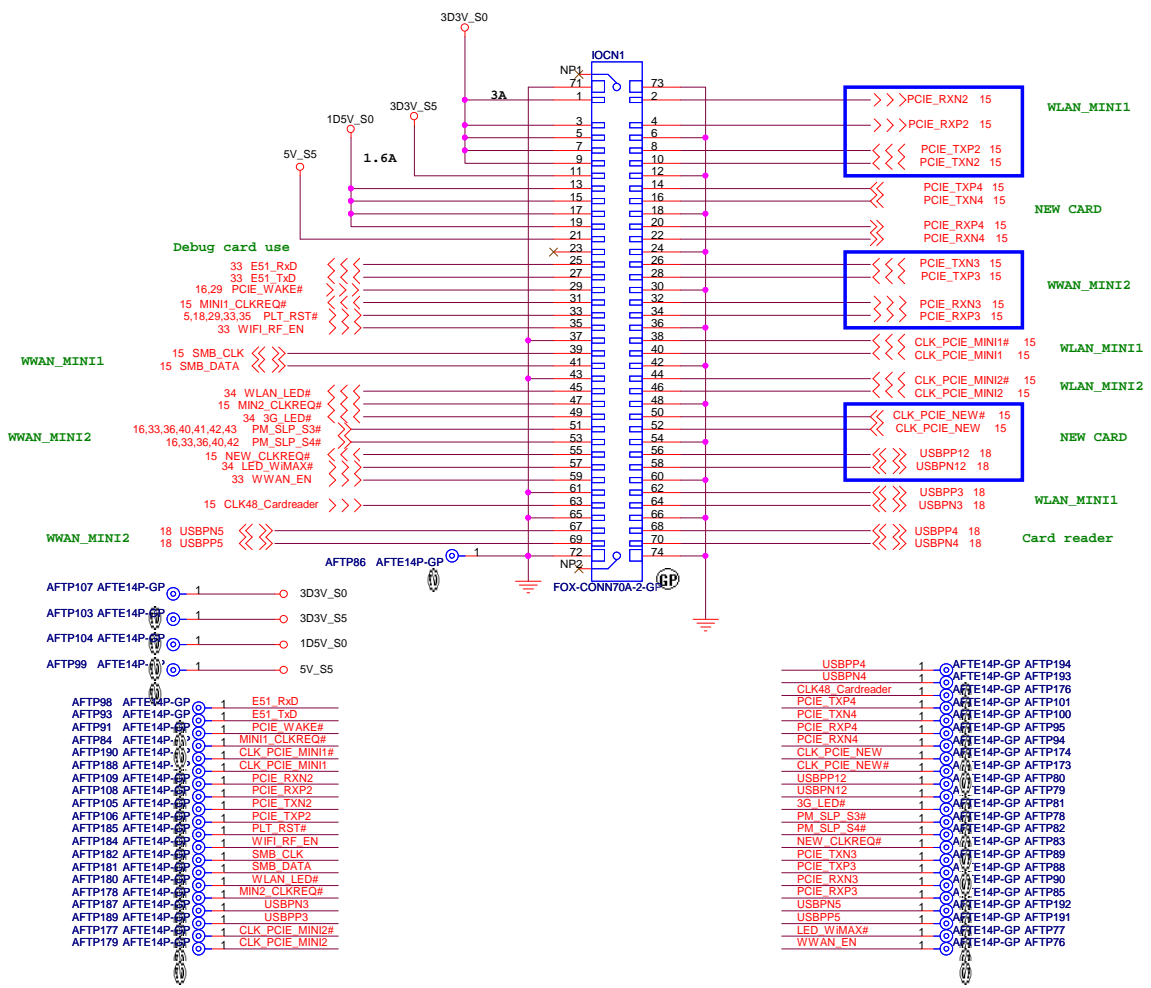
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1

MOVE MINI CARD TO I/O BOARD

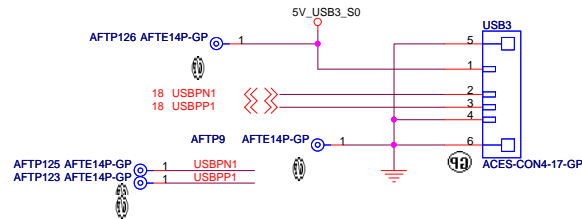


USBPP4	1	AFTP14P-GP	AFTP194
USBPN4	1	AFTP14P-GP	AFTP193
CLK48_Cardreader	1	AFTP14P-GP	AFTP176
PCIE_TXP4	1	AFTP14P-GP	AFTP101
PCIE_TXN4	1	AFTP14P-GP	AFTP100
PCIE_RXP4	1	AFTP14P-GP	AFTP95
PCIE_RXN4	1	AFTP14P-GP	AFTP94
CLK_PCIE_NEW	1	AFTP14P-GP	AFTP174
CLK_PCIE_NEW#	1	AFTP14P-GP	AFTP173
USBPP12	1	AFTP14P-GP	AFTP90
USBPN12	1	AFTP14P-GP	AFTP79
3G_LED#	1	AFTP14P-GP	AFTP81
PM_SLP_S3#	1	AFTP14P-GP	AFTP78
PM_SLP_S4#	1	AFTP14P-GP	AFTP82
NEW_CLKREQ#	1	AFTP14P-GP	AFTP83
PCIE_TXN3	1	AFTP14P-GP	AFTP89
PCIE_TXP3	1	AFTP14P-GP	AFTP88
PCIE_RXN3	1	AFTP14P-GP	AFTP90
PCIE_RXP3	1	AFTP14P-GP	AFTP85
USBPN5	1	AFTP14P-GP	AFTP192
USBPP5	1	AFTP14P-GP	AFTP191
LED_WIMAX#	1	AFTP14P-GP	AFTP77
WWAN_EN	1	AFTP14P-GP	AFTP76

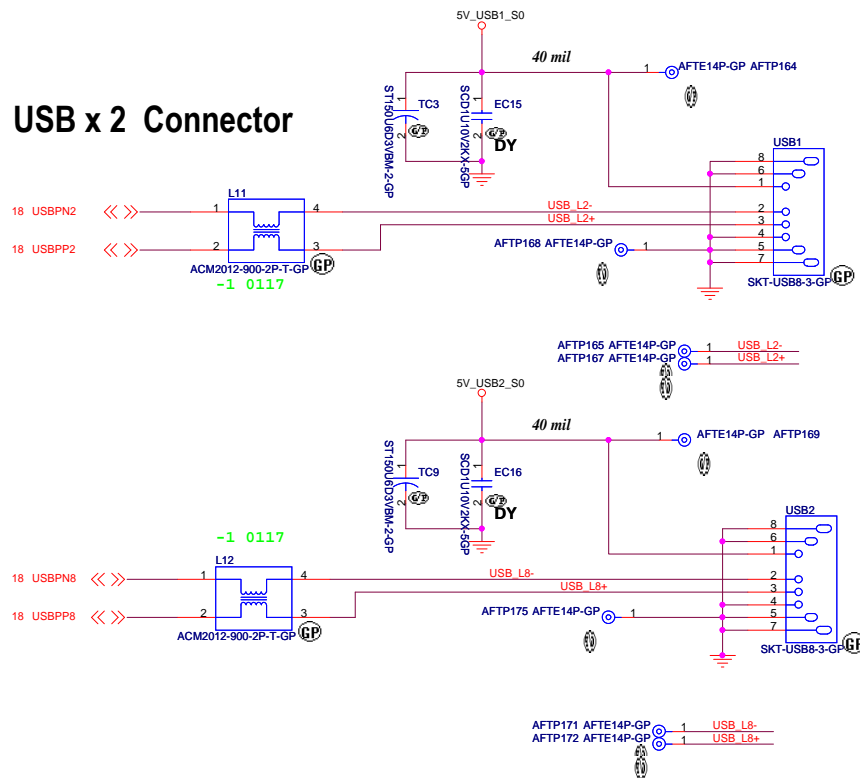
<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title	
IO CONN	
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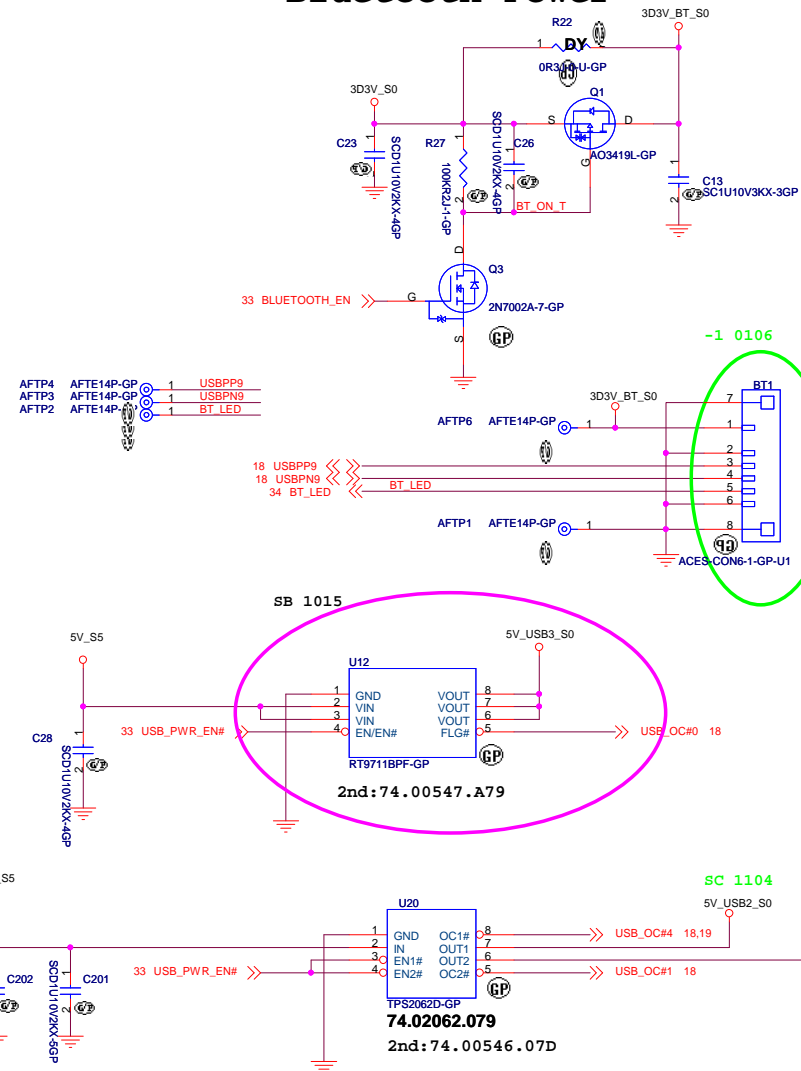
Should be in DC-IN board



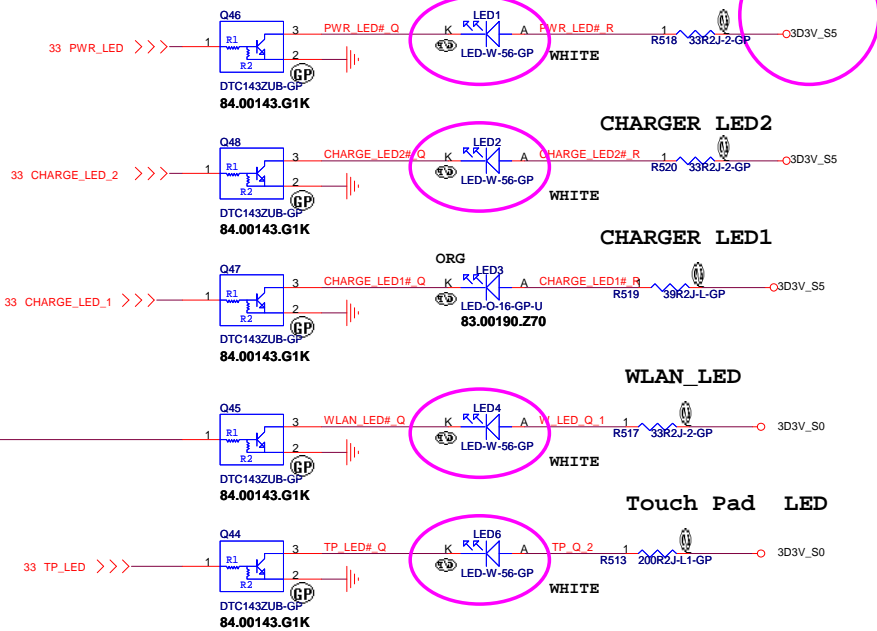
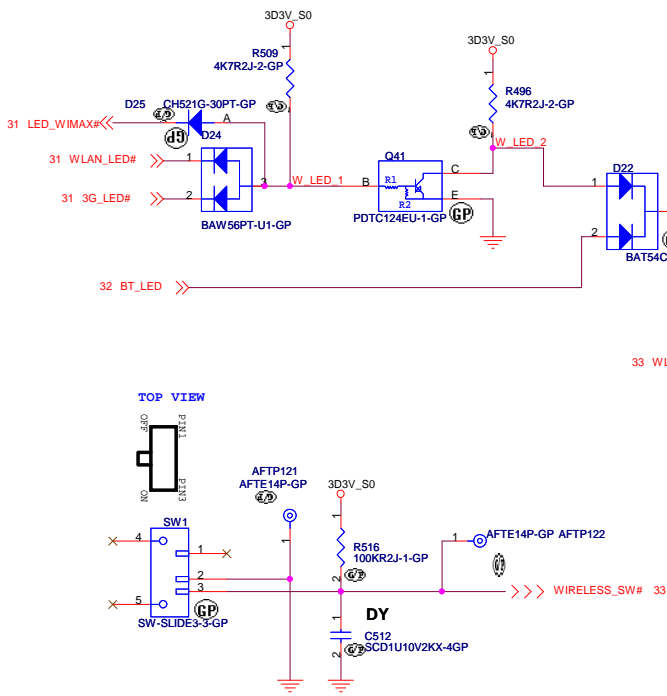
USB x 2 Connector



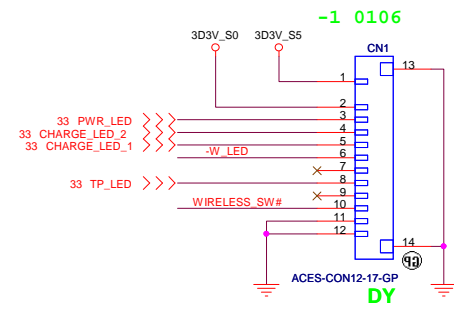
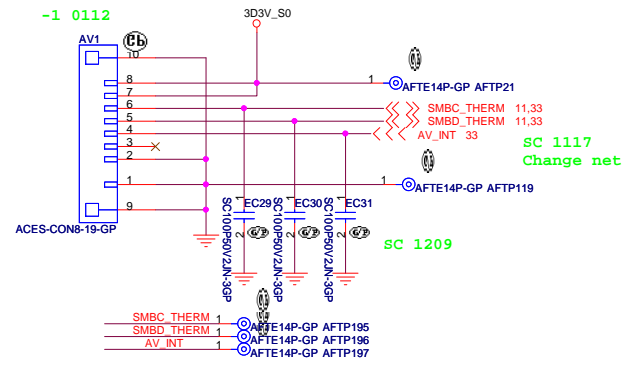
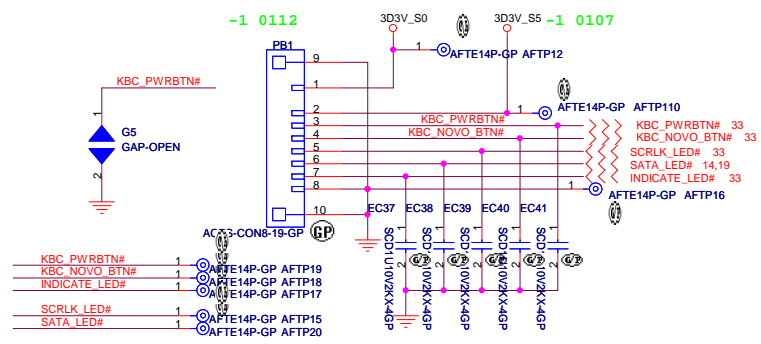
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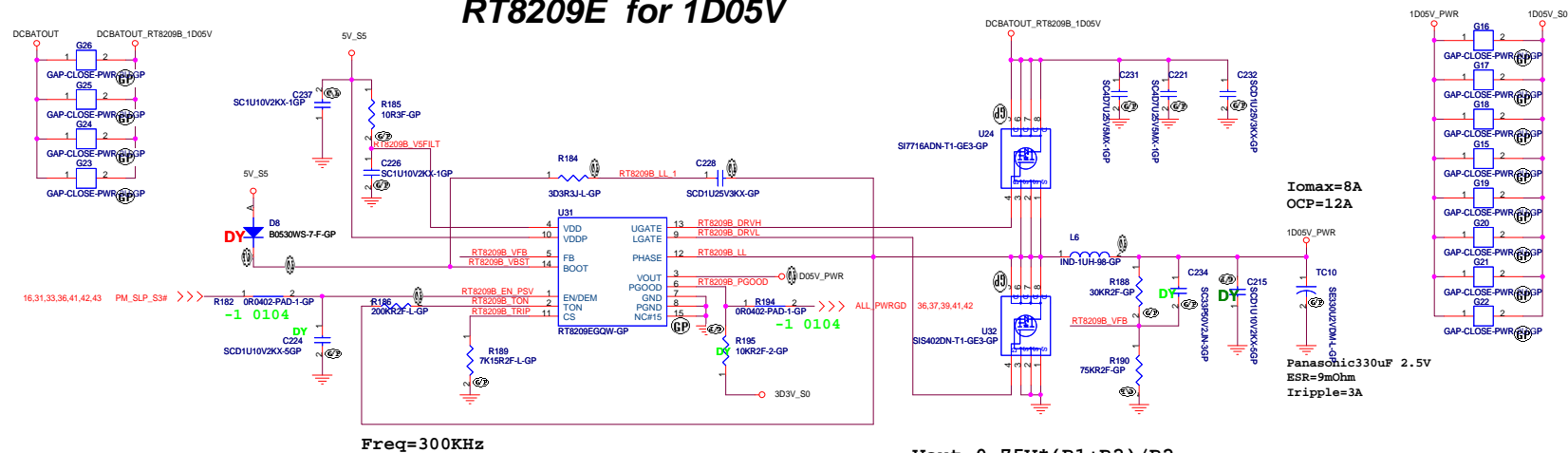
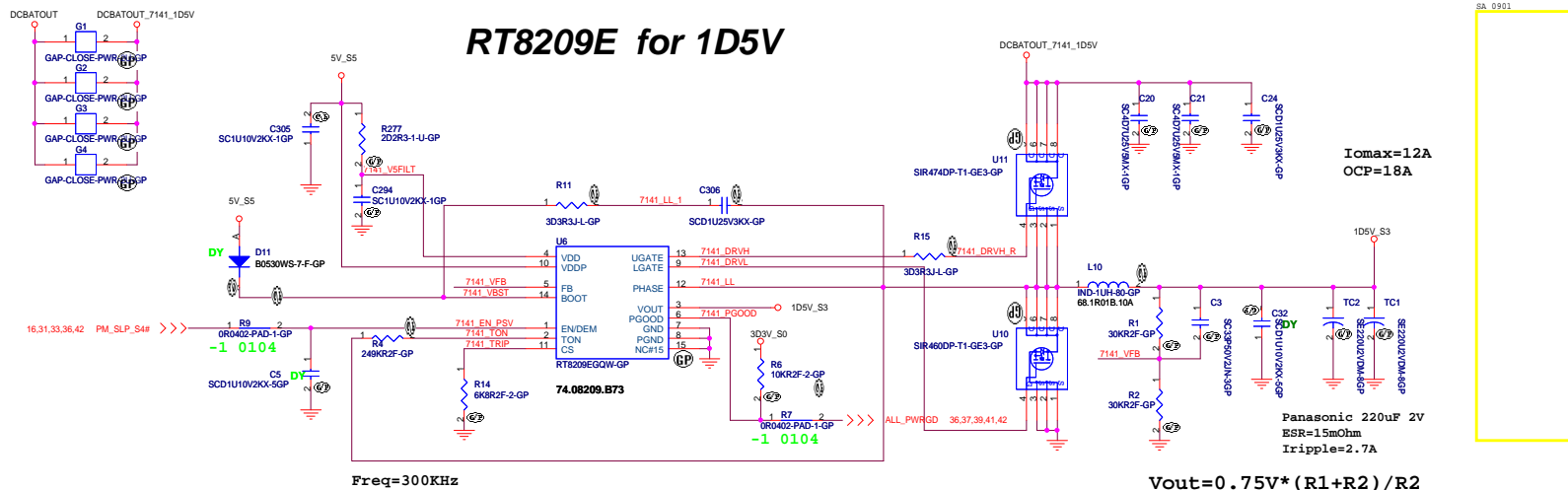




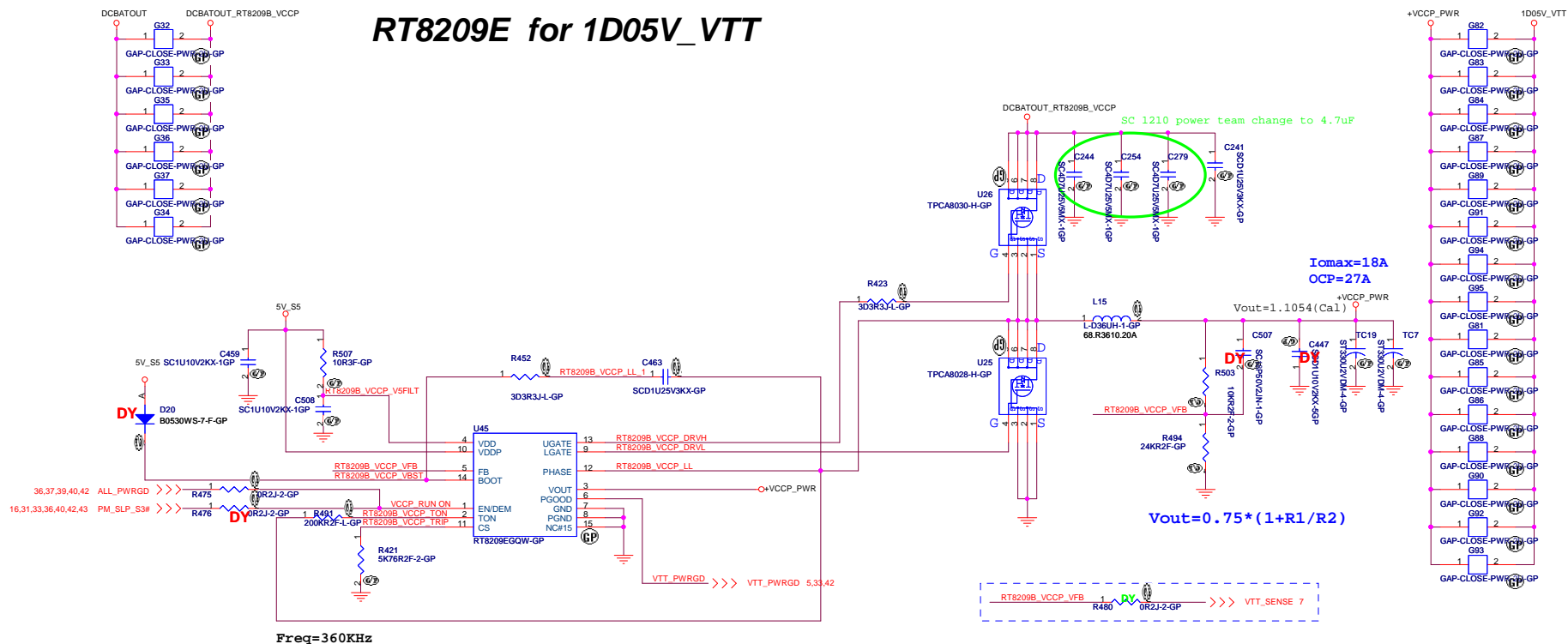
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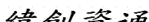


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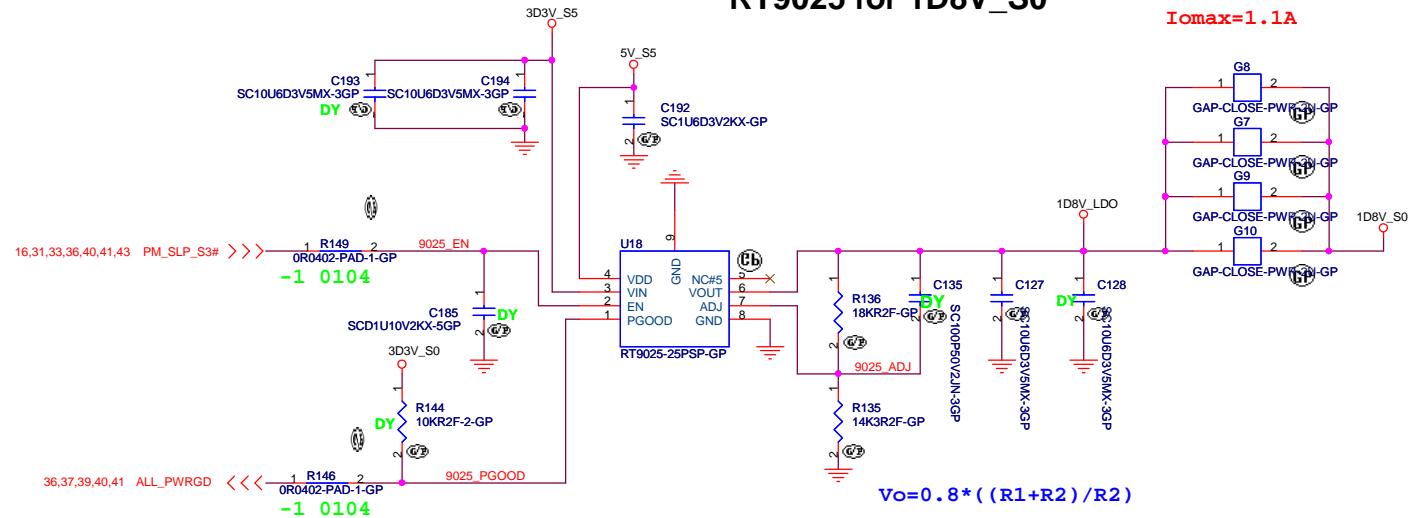


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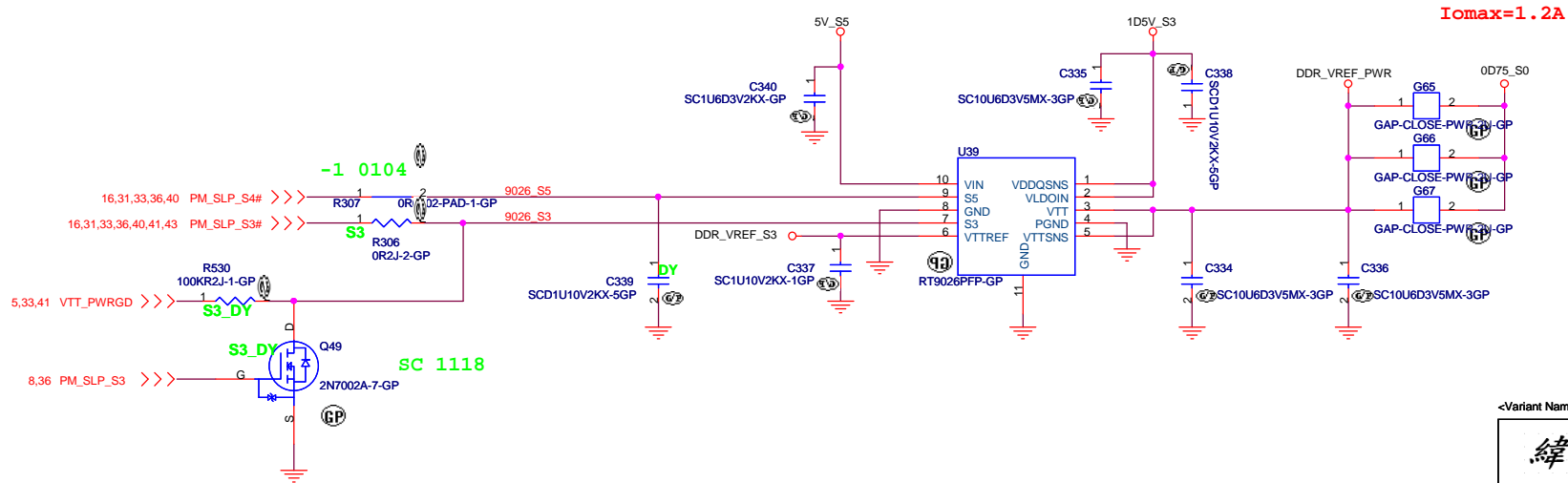


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RT9025 for 1D8V_S0



RT9026 for 0D75V_S3



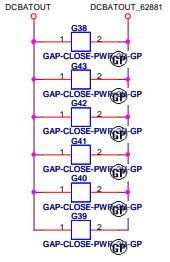
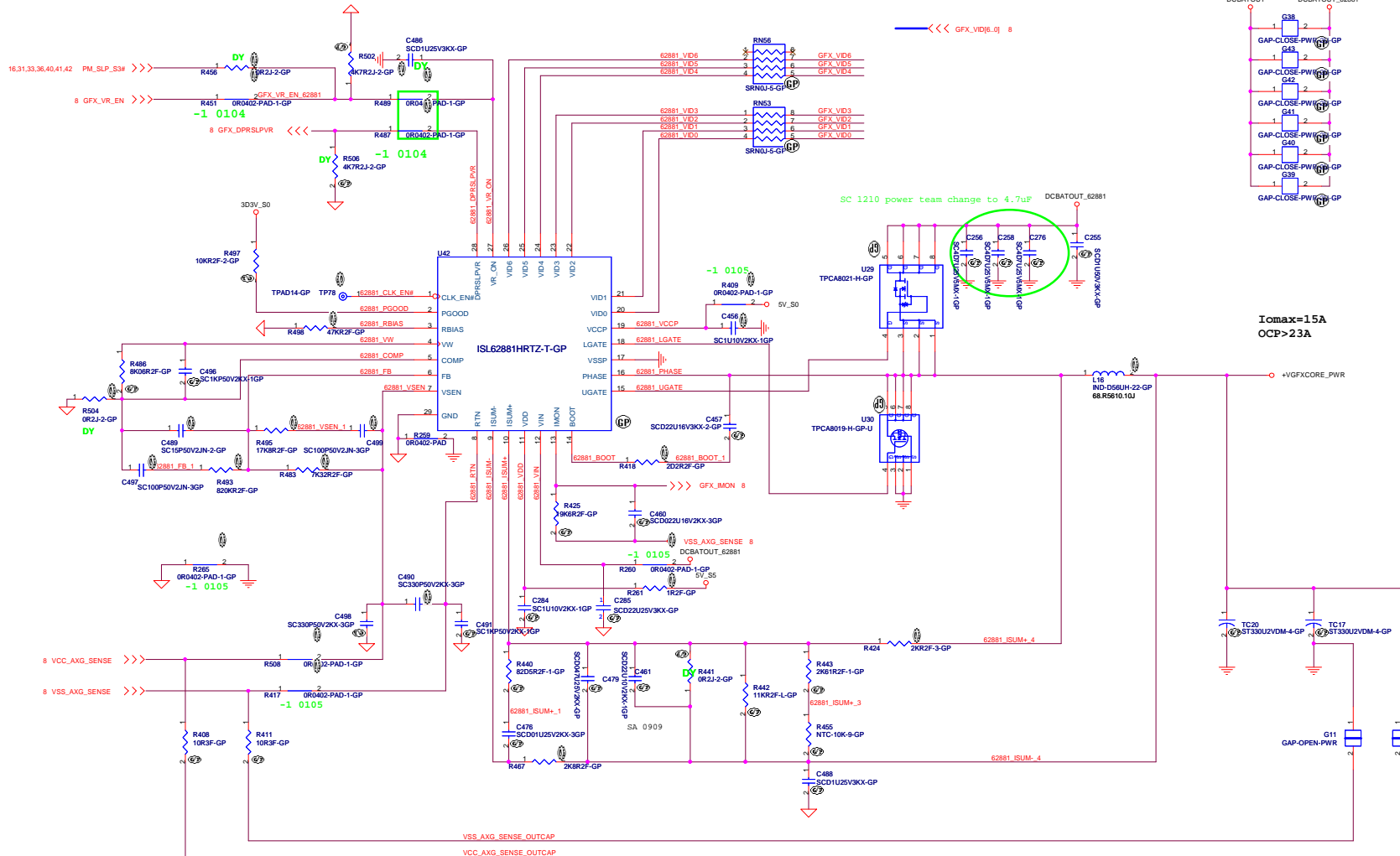
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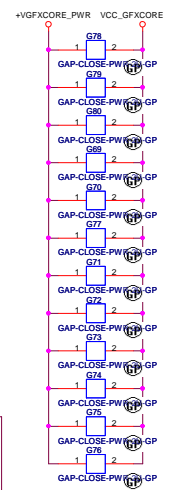
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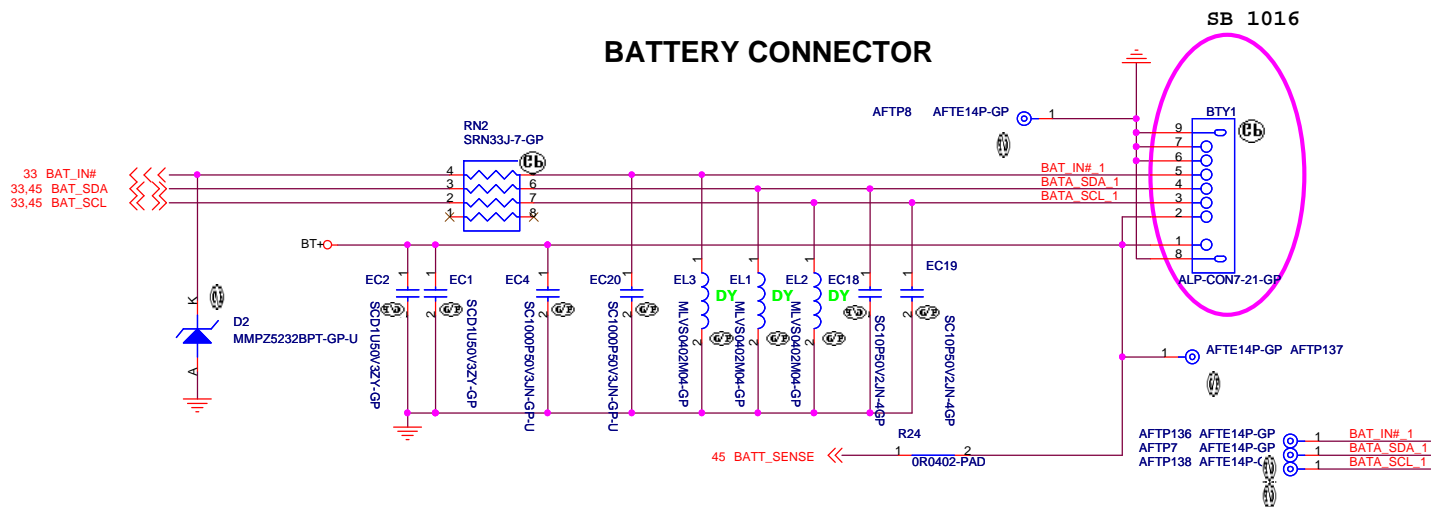
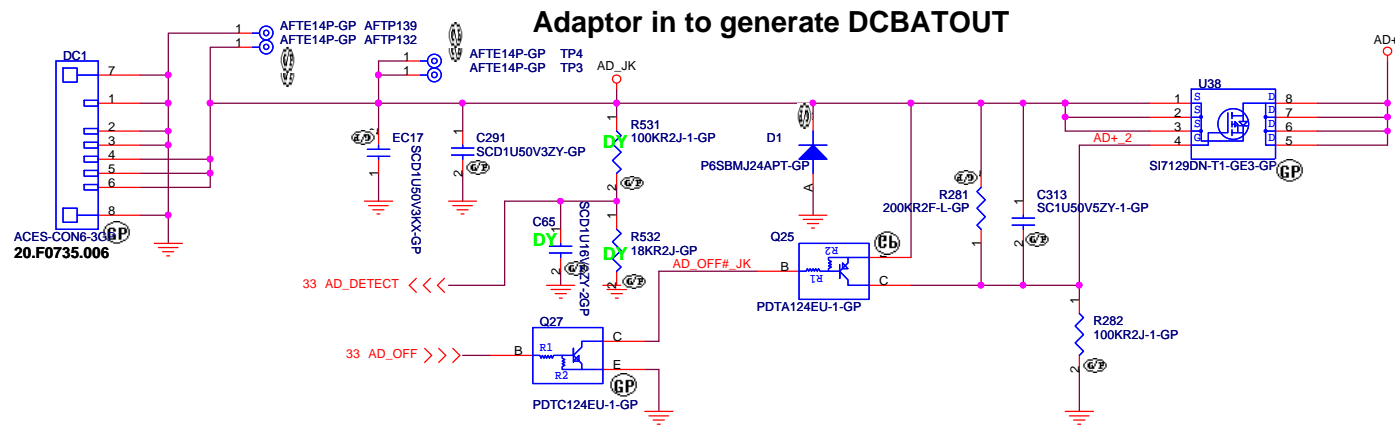
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